IJARCCE

ISSN (Online) 2278-1021
ISSN (Print) 2319 5940

International Journal of Advanced Research in Computer and Communication Engineering
ISO 3297:2007 Certified
Vol. 5, Issue 11, November 2016

Performance Enhancement in Combinational Circuit using Gate Diffusion Technique

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Abstract: Low power circuit design has been an important issue in VLSI design areas. Full adders are important components in application such as digital signal processors (DSP) and microprocessors. The full adder design can be designed by using conventional CMOS and positive feedback adiabatic logic (PFAL). The more number of transistors and more power can be needed. Gate diffusion technique (GDI) can be used to implement the full adder design. This technique allows the low power consumption and area of digital circuits while maintaining low complexity of logic design. In this work, the number of transistor and power of the conventional CMOS, positive feedback adiabatic logic (PFAL) and gate diffusion technique (GDI) are compared. Tanner EDA tool can be used for simulation.

Keywords: Full adder, multiplexer, conventional CMOS, Positive feedback adiabatic logic (PFAL), Gate diffusion input (GDI) technique.

I. INTRODUCTION

The primary issue in VLSI technology is low power, area, and high speed. Power minimization is important in today VLSI design methodologies because of two main reasons one is the long battery operating life requirement of mobile and other portable devices and second is due to increasing number of transistors in a single chip leads to high power dissipation and it can be lead to reliability and IC packaging problems. The energy dissipation in CMOS circuit is due to the charging and discharging of node capacitance of the circuits such as load capacitance and parasitic capacitance. Such part of the total power dissipated by the circuit is called dynamic power dissipation. In order to reduce the dynamic power dissipation, an alternative approach to the traditional CMOS technique of power consumption reduction, named adiabatic switching has been proposed. In adiabatic switching, the process of charging and discharging of node capacitance is carried out in such a way the small amount of power is wasted and the recovery of the energy stored on the capacitors is achieved.

The adiabatic circuits are low power circuits which use "reversible logic" to conserve energy. Unlike traditional CMOS circuits, which dissipate energy during switching, adiabatic circuits reduce dissipation by following two key rules (i) Never turn on a transistor when there is a voltage potential between the source and drain. (ii) Never turn off the transistor when current is flowing through it.

Adiabatic Logic is the term given to low power electronic circuits that implement reversible logic. The term comes from the fact that an adiabatic process is one in which the total heat or energy in the system remains constant. Research in this area has mainly; the circuits get smaller and faster. In this, the main design changes are focused in power clock which plays a vital role in the principle of operation.

A. Positive feedback adiabatic logic (PFAL):
The partial energy recovery circuit so called the positive feedback adiabatic logic (PFAL), The PFAL has been used, since its shows the lowest energy consumption and a good robustness against technical parameter variation. It is a dual rail circuit made by two PMOS and two NMOS that avoids a logic level degradation on the output node. The positive feedback adiabatic logic is shown in fig 1.

B. Gate diffusion input technique:
The basic GDI (gate diffusion input) cell consist of NMOS and PMOS as shown in fig 2. At first glance, the basic cell reminds the standard CMOS inverter, but there is some important differences.

(1) The GDI cell contains three input terminals- G(Common gate input of NMOS and PMOS), P(Input of the source/drain of PMOS) and N(Input of the source/drain of NMOS).
(2) In the GDI cell, the source of PMOS are not connected to Vdd and the source of NMOS is not connected to Gnd. This feature gives GDI cell two extra input pins for use.
(3) Bulk of both NMOS and PMOS are connected to N or P respectively, so it can be arbitrarily biased at contrast with CMOS inverter.

It must be remarked, that are not all the functions are possible in standard P-well CMOS process. But in the GDI technique can be successfully implemented on silicon on insulator (SOI) and twin-tub CMOS process. The basic GDI cell implementing the logic function is shown in table I.

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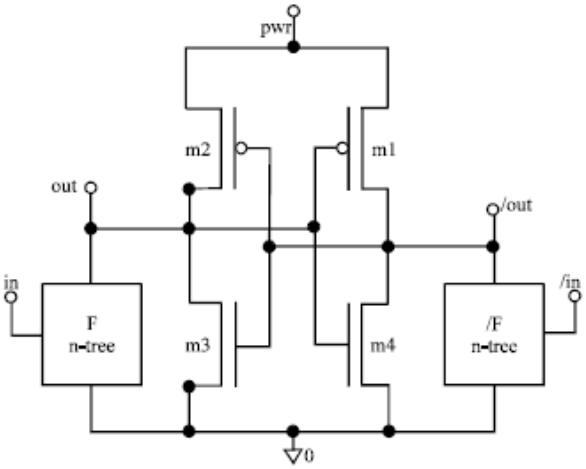

Fig. 1. Positive feedback adiabatic logic

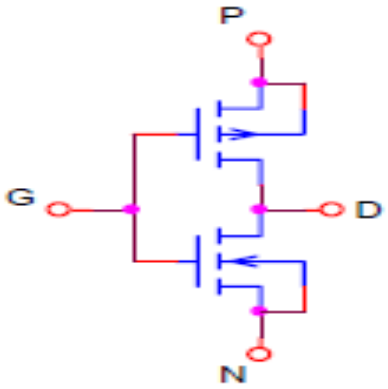

Fig. 1. Basic GDI cell

TABLE I Basic function using GDI cell

N	P	G	OUT	FUNCTION
0	B	A	A'B	F1
B	1	A	A'+B	F2
1	B	A	A+B	OR
B	0	A	AB	AND
C	B	A	A'B + AC	MUX
0	1	A	A'	NOT

II. CONVENTIONAL CMOS TECHNIQUE

A. FULL adder design

The basic cell in digital computing system is the 1-bit full adder which has 1-bit three inputs (A, B, Cin) and two 1-bit outputs(sum and carry). The full adder design using logic gates is shown in fig 3 and the truth table for full adder is shown is table II.

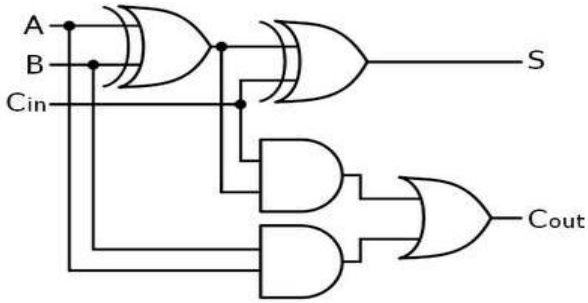

Fig. 3. Full adder using logic gates

TABLE II TRUTH TABLE FOR FULL ADDER DESIGN

A	B	C_{in}	Sum	C_{out}
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

The Boolean expression for full adder is given by

Sum=A xor B xor Cin

Carry=AB+BCin+ACin

The conventional CMOS full adder can be implemented using both pull-up network using PMOS transistors and pull-down network using NMOS transistors.

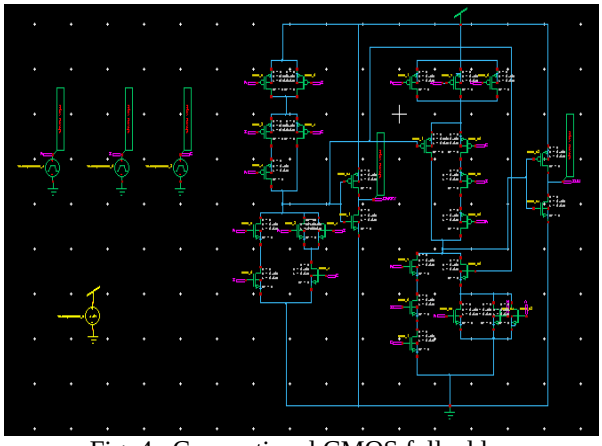

Fig. 4. Conventional CMOS full adder

B Multiplexer

A multiplexer is a device used to select one of the several analog or digital inputs. This input is then fed to the output line. The selection of the particular input depends on the select lines. A multiplexer with 2n inputs will have n select lines. The combination of these select lines determines the input which has to be routed to the output. A multiplexer is also known as data selector.

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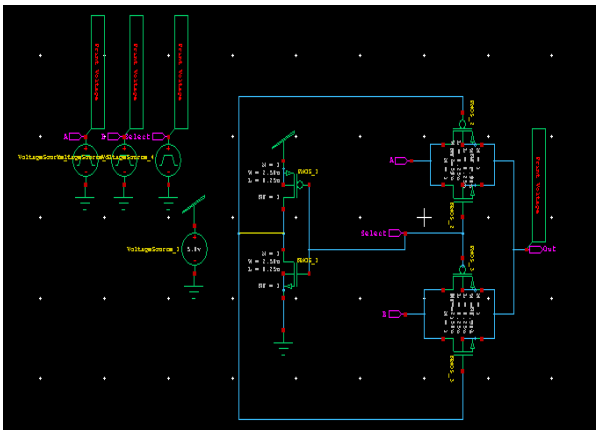

Fig 5. Conventional CMOS using multiplexer

III. POSITIVE FEEDBACK ADIABATIC LOGIC

A. full adder design

In the positive feedback adiabatic design full adder can be using only NMOS transistors and the two cross coupled inverters.

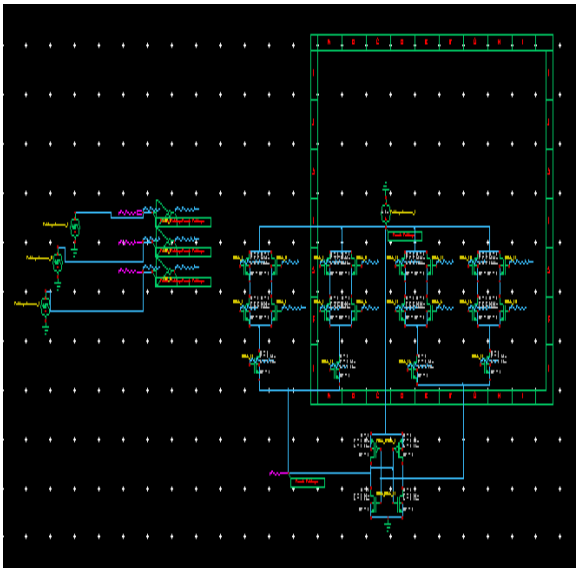

Fig.6. Positive feedback adiabatic logic using sum

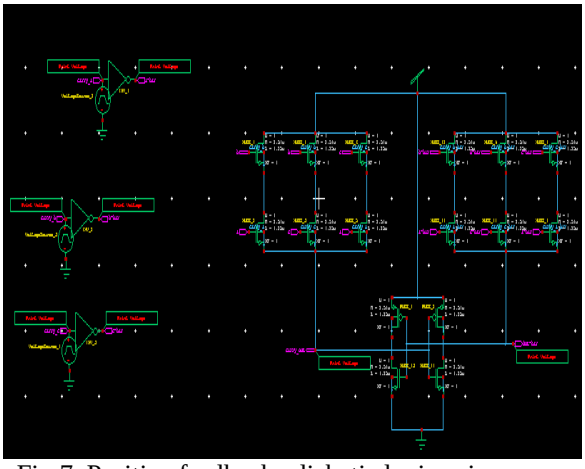

Fig.7. Positive feedback adiabatic logic using carry

B. Multiplexer

The positive feedback adiabatic logic using multiplexer is shown in fig 8. The multiplexer design can be implemented by using the NMOS transistors and two cross coupled inverters.

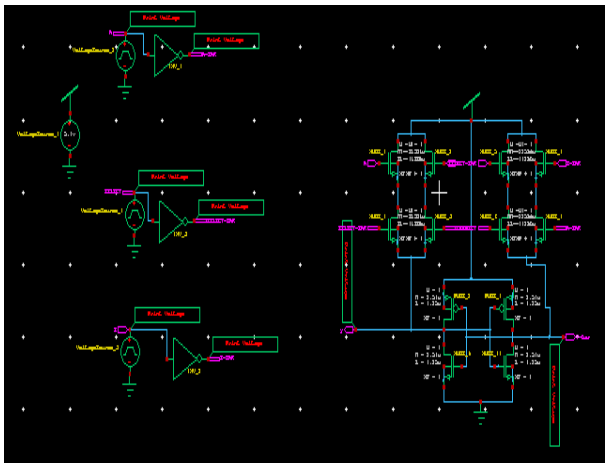

Fig. 8. Positive feedback adiabatic logic using multiplexer

IV. GATE DIFFUSION INPUT TECHNIQUE

A. Full adder design

The full adder can be implemented by using the gate diffusion technique is shown in fig 9. The full adder circuit is designed by using XOR gates and multiplexers.

The Boolean expression for full adders can be given by

Sum=A xor B xor C

Carry=AB+[A xor B]B

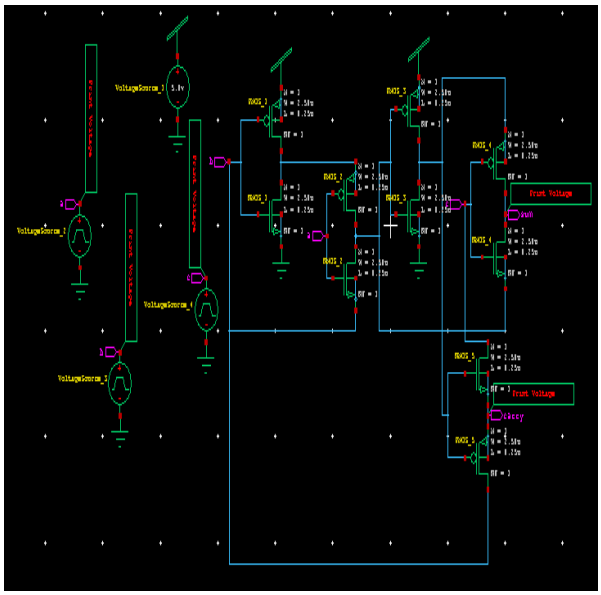

Fig. 9. GDI technique using full adder

B. Multiplexer

The multiplexer can be designed by using the gate diffusion technique. The one PMOS and one NMOS transistors can be used to designing the multiplexer.

DOI 10.17148/IJARCCE.2016.51153

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The Boolean expression for multiplexer can be given by

Out=A'B+AC

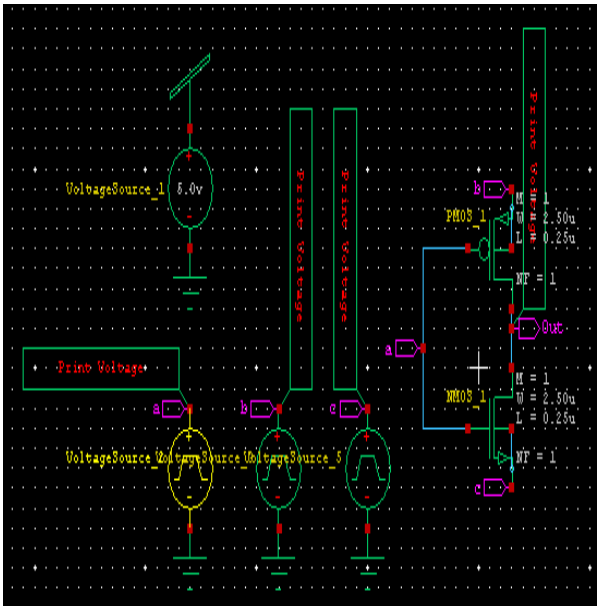

Fig. 10.GDI technique using multiplexer

V. SIMULATION RESULT

Performance analysis of full adder and multiplexer design using conventional CMOS, positive feedback adiabatic logic and GDI technique.

TABLE III comparison of full adder using conventional CMOS, positive feedback adiabatic logic and GDI technique

Circuit design	No. Of Transistor	Power
Conventional multiplexer	6	2.711625e-7
PFAL multiplexer	12	1.484799e-2
GDI multiplexer	2	2.50000e-11

TABLE IV Comparison of Multiplexer Using Conventional CMOS, Positive Feedback Adiabatic Logic And GDI Technique-

Circuit design	No. Of transistors	Power
Conventional CMOS full adder	28	1.363191e-6
PFAL full adder sum	24	2.464038e-6
PFAL full adder carry	16	3.261662e-2
GDI full adder	10	1.287068e-6

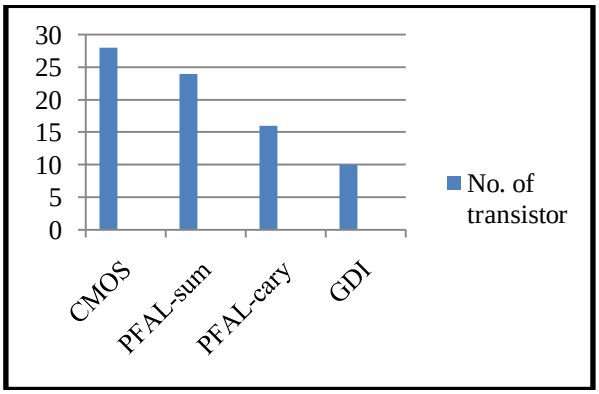

Fig. 11. Comparison of full adder for No. of transistor and power

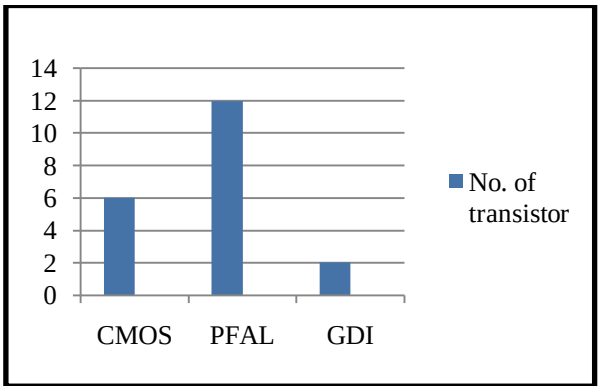

Fig. 12. Comparison of multiplexer for No. of transistor and power

VI. CONCLUSION

We can compare the performance of the different technique such as conventional CMOS, positive feedback adiabatic logic and gate diffusion input(GDI) technique using full adder and multiplexer design. For the comparison table, the power can be reduced in the gate diffusion technique. It is also most effective in terms of number of transistors required. So, the GDI technique is better than conventional CMOS and PFAL techniques in terms of power consumption and area (Number of transistor).

VII. FUTURE SCOPE

Future work will be focused on reduction of power and area in any combinational circuit and sequentional circuit using GDI technique.

REFERENCES

[1] Sakshi Goyal and Gurvinder Singh, Pushpinder Sharma, "Variation of Power Dissipation for Adiabatic CMOS and Conventional CMOS Digital Circuits" in ieee sponsored 2nd international conference on electronics and communication system (ICECS 2015)

[2] Arunkumar, and Manoj Sharma "Design and analysis of MUX using adiabatic technique ECRL and PFAL," in International

Conference on Advances in Computing,Communications and Informatics, 2013.
[3] R.Swapna, Shoban Mude "Adiabatic Implementation on Full Adder Circuits " in Int. Journal of Engineering Research and Applications , 2013
[4] Monika Sharma , " Design and Analysis of CMOS Cells using Adiabatic Logic" in International Journal of Networks and systems, 2012.
[5] Kunal & Nidhi kedia "A Power- efficient method for digital circuits", International Journal of Advanced Electrical and Electronics Engineering, (IJAEEE), ISSN (Print): 2278-8948, Volume-1, Issue-3, 2012
[6] Arkadiy morgenhtein, Idan Shwartz and Alexander fish "Gate diffusion input(GDI) logic 9n standard CMOS nanoscale process", 2010 IEEE 26th convention of Electrical and Electronics Engineering in Isreal.
[7] Bhaskar Uma Mahesh "Design and analysis of Full adders using adiabatic logic", Journal of Innovation in Computer science and Engineering Vol.3(1), Jul-Dec 2013.
[8] Gorpreet Kaur and Narinder Sharma "Comparison of adiabatic and conventional CMOS", nternational Journal of Computer Techniques, Vol.1 Issue 2 Dec-2014
[9] S.Abirami, M.Arul Kumar,E.Abinaya, J. Sowmya, "Design and analysis of 2:1 multiplexer circuits for high performance" International Jpurnal of Electrical and Electronics Engineers(IJEEE) Vol.No. 7, issue No. 01, Jan-Jine 2015
[10] Mishahsaad and Sangeeta mangesh,"Design of low power CMOS inverter using forced NMOS approach" International Journal of Scientific and Engineering Research, ISSN 2229-5518, Vol. 4 issue 7, July 2013.
[11] Gupta, Neha arora, Dr. B.P. Singh, "Design and analysis of 2:1 multiplexer for performance digital systems" International Journal of Electronics and Communication Technology(IJECT), Vol.3,issue 1, Jan-Mar 2012.
[12] Arkadiy morgenshtein, Alexander Fish and Isreal A. wagner, "Gate-diffusion input(GDI)- A technique for low power design of digital circuits: Analysis and Performance" IEEE-2002.
[13] Mukesh Tiwari, Jaikaran Singh, Yashasvi Vaidhya, "Adiabatic positive feedback charge recovery logic for low power CMOS design", International Journal of Computer Technology and Electronics Engineering(IJCTEE) Vol 2, issue 5, October 2012.
[14] Mr.Gawav Kumar, Atal S.M.Tripathi, "Design and simulation of CMOS cells using adiabatic technique for low power consumption", International Journal of Engineering and Technical Research-2014.
[15] W.C. Athas, L.Svsensson, J.F. Koller, N.Tzartzanis, and E.Y. Chou, "Low-power Digital systems based on adiabatic-switching principles", IEEE Transaction on very large scale integration(VSI) systems, 2(4),1994,398-407.
[16] A.Vetuli S.D.Pascolli and L.M.Revneri, "Positive feedback in adiabatic logic", IEEE Elecronics letters,32(20),1996,1887-1869.
[17] Study of Existing Full Adders and To Design a LPFA (Low Power Full Adder)", International Journal of Engineering Research and Applications (IJERA) ISSN: 2248-9622 Vol. 3, Issue 3, May-Jun 2013, pp.509-513
[18] P.Teichmann, "Adiabatic logic", Springer series in advanced microelectronics, 34,2012 .
[19] A. Blotti, S.Di Pascoli and R.Saletti,"Simple model for positive feedback adiabatic logic power consumption estsimation", IEEE Electronics letters, 36(2),2000,116-118.
[20] Y.Sunil Gavaskar Reddy and V.V.G.S. Rajendra Prasad, "Power comparison of CMOS and adiabatic full adder circuits".
[21] Pardeep Kumar, Susmita Mishra, Amrita Singh, "Study of existing full adders and to design LPFA(low power full adder)", International Journal of Engineering Research and Applications(IJERA), ISSN:2248-9622, Vol. 3, issue 3, May-Jun 2013,pp.509-51.